proceeds to 845. In step 845, it conveys status stored in the status register back to status is conveyed to the message engine 315 state machine 410.

Referring again to FIG. 7, the interrupt control status register 412 will be described in more detail. As described above, a packet is sent by the pocketsize portion of the packetizer/de-packetizer 428 to the crossbar switch 320 for transmission to one or more of the directors. It is to be noted that the packet sent by the packetizer portion of the packetizer/de-packetizer 428 passes through a parity generator PG in the message engine 315 prior to passing to the crossbar switch 320. When such packet is sent by the message engine 315 in exemplary director 180_1, to the crossbar switch 320, a parity bit is added to the packet by parity bit generator PG prior to passing to the crossbar switch 320. The parity of the packet is checked in the parity checker portion of a parity checker/generator (PG/C) in the crossbar switch 320. The result of the check is sent by the PG/C in the crossbar switch 320 to the interrupt control status register 412 in the director 180_1.

Likewise, when a packet is transmitted from the crossbar switch 320 to the message engine 315 of exemplary director 180_1, the packet passes through a parity generator portion of the parity checker/generator (PG/C) in the crossbar switch 320 prior to being transmitted to the message engine 315 in director 180_1. The parity of the packet is then checked in the parity checker portion of the parity checker (PC) in director 180_1 and is the result (i.e., status) is transmitted to the status register 412.

A number of embodiments of the invention have been described. Nevertheless, it will be understood that various modifications may be made without departing from the spirit and scope of the invention. Accordingly, other embodiments are within the scope of the following claims.

WHAT IS CLAIMED IS:

1. A system interface comprising:

a plurality of first directors;

a plurality of second directors;

a data transfer section having a cache memory, such cache memory being coupled to the plurality of first and second directors;

a messaging network, operative independently of the data transfer section, coupled to the plurality of first directors and the plurality of second directors; and

wherein the first and second directors control data transfer between the first directors and the second directors in response to messages passing between the first directors and the second directors through the messaging network to facilitate data transfer between first directors and the second directors with such data passing through the cache memory in the data transfer section.

2. The system interface recited in claim 1 wherein each one of the first directors includes:

a data pipe coupled between an input of such one of the first directors and the cache memory;

a controller for transferring the messages between the message network and such one of the first directors.

3. The system interface recited in claim 1 wherein each one of the second directors includes:

a data pipe coupled between an input of such one of the second directors and the cache memory;

a controller for transferring the messages between the message network and such one of the second directors.

4. The system interface recited in claim 2 wherein each one of the second directors includes:

a data pipe coupled between an input of such one of the second directors and the cache memory;

a controller for transferring the messages between the message network and such one of the second directors.

5. The system interface recited in claim 1 wherein each one of the first directors includes:

a data pipe coupled between an input of such one of the first directors and the cache memory;

a microprocessor; and

a controller coupled to the microprocessor and the data pipe for controlling the transfer of the messages between the message network and such one of the first directors and for controlling the data between the input of such one of the first directors and the cache memory.

6. The system interface recited in claim 1 wherein each one of the second directors includes:

a data pipe coupled between an input of such one of the second directors and the cache memory;

a microprocessor; and

a controller coupled to the microprocessor and the data pipe for controlling the transfer of the messages between the message network and such one of the second directors and for controlling the data between the input of such one of the second directors and the cache memory.

7. The system interface recited in claim 5 wherein each one of the second directors includes:

a data pipe coupled between an input of such one of the second directors and the cache memory;

a microprocessor; and

a controller coupled to the microprocessor and the data pipe for controlling the transfer of the messages between the message network and such one of the second directors and for controlling the data between the input of such one of the second directors and the cache memory.

8. A data storage system for transferring data between a host computer/server and a bank of disk drives through a system interface, such system interface comprising:

a plurality of first directors coupled to host computer/server;

a plurality of second directors coupled to the bank of disk drives;

a data transfer section having a cache memory, such cache memory being coupled to the plurality of first and second directors;

a messaging network, operative independently of the data transfer section, coupled to the plurality of first directors and the plurality of second directors; and

wherein the first and second directors control data transfer between the host computer and the bank of disk drives in response to messages passing between the first directors and the second directors through the messaging network to facilitate the data transfer between host computer/server and the bank of disk drives with such data passing through the cache memory in the data transfer section.

9. The system interface recited in claim 8 wherein each one of the first directors includes:

a data pipe coupled between an input of such one of the first directors and the cache memory;

a controller for transferring the messages between the message network and such one of the first directors.

10. The system interface recited in claim 8 wherein each one of the second directors includes:

a data pipe coupled between an input of such one of the second directors and the cache memory;

a controller for transferring the messages between the message network and such one of the second directors.

11. The system interface recited in claim 9 wherein each one of the second directors includes:

a data pipe coupled between an input of such one of the second directors and the cache memory;

a controller for transferring the messages between the message network and such one of the second directors.

12. The system interface recited in claim 8 wherein each one of the first directors includes:

a data pipe coupled between an input of such one of the first directors and the cache memory;

a microprocessor; and

a controller coupled to the microprocessor and the data pipe for controlling the transfer of the messages between the message network and such one of the first directors and for controlling the data between the input of such one of the first directors and the cache memory.

13. The system interface recited in claim 8 wherein each one of the second directors includes:

a data pipe coupled between an input of such one of the second directors and the cache memory;

a microprocessor; and

a controller coupled to the microprocessor and the data pipe for controlling the transfer of the messages between the message network and such one of the second directors and for controlling the data between the input of such one of the second directors and the cache memory.

14. The system interface recited in claim 12 wherein each one of the second directors includes:

a data pipe coupled between an input of such one of the second directors and the cache memory;

a microprocessor; and

a controller coupled to the microprocessor and the data pipe for controlling the transfer of the messages between the message network and such one of the second directors and for controlling the data between the input of such one of the second directors and the cache memory.

15. A method for operating a data storage system adapted to transfer data between a host computer/server and a bank of disk drives, such method comprising:

transferring messages through a messaging network with the data being transferred between the host computer/server and the bank of disk drives through a cache memory, such message network being independent of the cache memory.

16. A method of operating a data storage system adapted to transfer data between a host computer/server and a bank of disk drives through a system interface, interface comprising: a plurality of first directors coupled to host computer/server; a plurality of second directors coupled to the bank of disk drives; and a data transfer section having a cache memory, such cache memory being coupled to the plurality of first and second directors, such method comprising:

transferring the data between the host computer/server and the bank of disk drives under control of the first and second directors in response to messages passing between the first directors and the second directors through a messaging network to facilitate the data transfer between host computer/server and the bank of disk drives with such data passing through the cache memory in the data transfer section, such message network being independent of the cache memory.

17. A method of operating a system interface having a plurality of first directors, a plurality of second directors and a data transfer section having a cache memory, such cache memory being coupled to the plurality of first and second directors, such method comprising:

providing a messaging network, operative independently of the data transfer section, coupled to the plurality of first directors and the plurality of second directors to control data transfer between the first directors and the second directors in response to messages passing between the first directors and the second directors through the messaging network to facilitate data transfer between first directors and the second directors with such data passing through the cache memory in the data transfer section.

18. The method recited in claim 17 including providing each one of the first directors is provided with:

a data pipe coupled between an input of such one of the first directors and the cache memory;

a controller for transferring the messages between the message network and such one of the first directors.

19. The method recited in claim 17 including providing each one of the second directors with:

a data pipe coupled between an input of such one of the second directors and the cache memory;

a controller for transferring the messages between the message network and such one of the second directors.

20. The method recited in claim 18 including providing each one of the second directors with:

a data pipe coupled between an input of such one of the second directors and the cache memory;

a controller for transferring the messages between the message network and such one of the second directors.

21. The method recited in claim 17 including providing each one of the first directors with:

a data pipe coupled between an input of such one of the first directors and the cache memory;

a microprocessor; and

a controller coupled to the microprocessor and the data pipe for controlling the transfer of the messages between the message network and such one of the first directors and for controlling the data between the input of such one of the first directors and the cache memory.

22. The method recited in claim 17 including providing each one of the second directors with:

a data pipe coupled between an input of such one of the second directors and the cache memory;

a microprocessor; and

a controller coupled to the microprocessor and the data pipe for controlling the transfer of the messages between the message network and such one of the second directors and for controlling the data between the input of such one of the second directors and the cache memory.

23. The method recited in claim 21 including providing each one of the second directors with:

a data pipe coupled between an input of such one of the second directors and the cache memory;

a microprocessor; and

a controller coupled to the microprocessor and the data pipe for controlling the transfer of the messages between the message network and such one of the second directors and for controlling the data between the input of such one of the second directors and the cache memory.

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